CSPs Assembly Reliability

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology

Abstract

Availability of board solder joint reliability information is critical to the wider implementation of Chip Scale Packages (CSPs). This paper will compare three different CSPs concepts as well as their assembly reliability. In addition, literature cycling data for solder joint reliability of several low pin count packages will be projected for a specific environment using a modified Coffin-Manson relationship. Projected reliability results presented in graphs will be compared to the thermal cycling test results generated at JPL for low I/O leadless ceramic packages.

Introduction

In surface mount technology (SMT), electronic packages are mounted and terminated directly onto the PWB surface rather than inserting the leads into plated through-holes (PTHs). There are several surface mount package styles, both active and passive. Active devices are divided into those with terminations of leads on the periphery of the component, two sides or four sides, or those with terminations (either pads or solder bumps) over much of the bottom of the component. Peripheral Array Packages (PAP) have less potential for significant reduction in size in conjunction with increase in I/O counts compares to Area Array Packages (AAPs). The BGAs from the latter category are now the mainstay alternative.

For example, the CSP version of two sided PAP are the Lead-On-Chip (LOC) packages and the versions for PAP are micro- (or mini-)BGA packages with generally eutectic balls.

Another level of miniaturization is accomplished by directly attaching the bare die on the PWB. The direct Flip Chip On Board (FCOB) is the ultimate miniaturization level achieving nearly 70% efficient use of the area of the die ratio to the PWB's foot print. In FCOB, solder bumps are permanently attached to the face of bare die, the flip side is mounted on the PWB. In Chip-On-Board, with about 50% use of area efficiency, the pads of wire bonded are used for second level wire bonding onto the PWB.

Chip Scale Packages

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are now at the stage Ball Grid Arrays (BGAs) were about two years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages.

CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die, respectively. Many manufacturers now refer to CSPs as packages that are the miniaturized version of their previous generation. Two concepts of CSPs are shown in Figure 1. Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes

- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPS do not permit significant redistribution and the current cost effective PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- Protects the dic from physical and alpha radiation damages, and provides a vehicle for thermal dissipation and case of dic functionality testing.

CSPS generally have been categorized based on their fundamental structures These arc:

- Interposer packages with either flex or rigid substrate
- Wafer level molding and assembly redistribution
- Lead On Chip (LOC) packages.

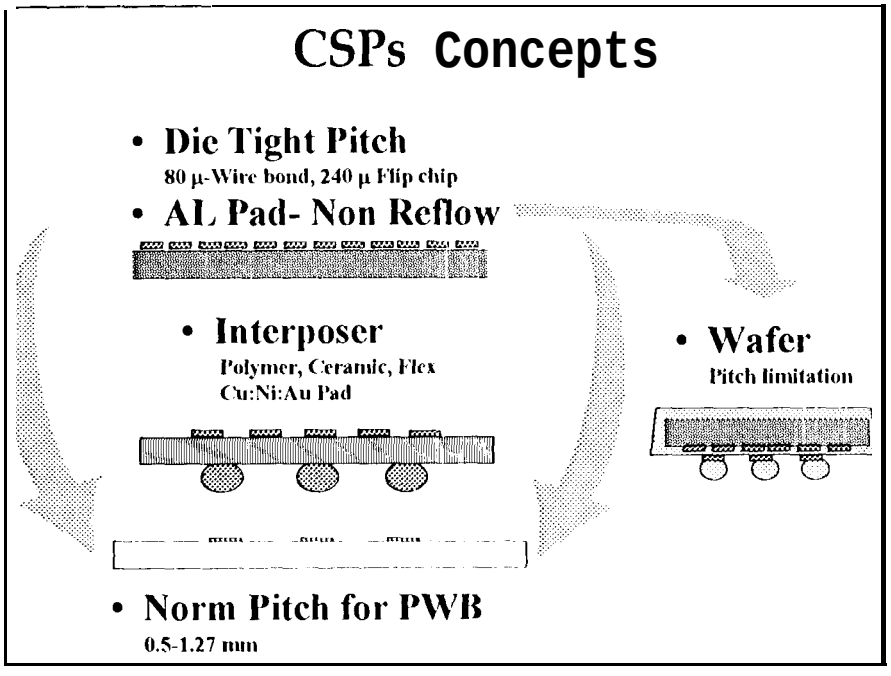


Figure 1: **Two** Chip Scale Package Concepts

CSPs Assembly Reliability

Currently, most of data arc those that were generated for package qualifications by manufacturers with very limited published information available 011 assembly reliability. These data arc of limited value to the end user since often they have been collected under significantly different manufacturing and environmental conditions or for packages with di fferent pin counts.

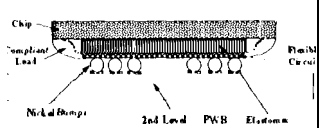
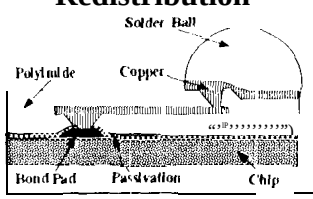
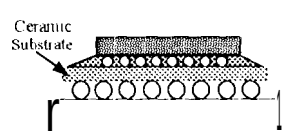
Failure at the board level could caused by either the failure of (1IC package itself 01 the package to board connection, The latter could be caused by the intrinsic wear-out mechanism or by hostile environmental factors. The thermo-mechanical wear (creep) of solder joints is the cause of failure of most CSP assemblies. Failure of solder joint can be caused by mechanical stresses in a non-uniform thermal expansion and/or contraction of different materials in the assembly. To achieve minimum damage to solder joints, thermal mismatch between the die and board should be minimized either by package optimizing or appropriate bard material selection. Only a few of the CSP packages have been designed to alleviate damage due to the thermal expansion of package/board mismatches.

Literature Data on CSP Assembly Reliability

Table 1 lists the assembly reliability for flex or rigid interposers, and wafer level packages. Aspects of cycling conditions with their failure mechanisms arc summarized in the following:

- CTE absorbed CSP: Thermal cycling test results for a coefficient of thermal expansion (CTE) mismatched relieved package arc shown in the Table 1. This package uses a TAB-like IC interconnects, a resilient elastomeric interposer, and eutectic solder balls. The resilient interposer in conjunction with springiness of TAB interconnection cause to alleviate thermal expansion differences between the chip (CTE 2-3 ppm/°C) and PWB (CTE for FR-4 -15 ppm/°C). This package has shown to be reliable, robust, and 00 requirement for underfilling. Thermal cycling/shock data given in the Table were for daisy chain packages on FR-4 and were performed from the liquid nitrogen temperature (- 196°C) to hot oil (160°C). Because of low strain state of solder joints, wear out failure mechanism of solder joints were not observed and failure was shifted to the heel of TAB interconnection with high mismatched stress levels. Significant improvement was observed when ductile gold leads were used. The gold version showed no failure up to 2000 cycles in the range of -65°C to 150°C. The thermal cycling screening test results with assembly exposures to extremely low (stress conditions) and high temperatures (strain conditions) arc not realistic and their failure mechanisms might not be representative of those of field failure. Onc such failure due to extreme high temperature exposure is the chambering and deformation of FR-4 close to its glass transition temperature (Tg). The PWB materials will show severe damage if cycling temperature become close or exceeds their glass transition temperatures, the temperature that polymer materials starts to become soft. Indeed, it was observed that FR-4 plated through holes had massive barrel cracking failure.

Table 1. Literature data on CSPs assembly Reliability

Package Type Schematic (not to scale)	Cycling Condition	Total Cycles	Fails/ Samples	1/0	References (comments)
Flex interposer CTE matched 	-1 96°C<>160°C -65°C<>150°C	130 no underfill 1163 2000*	0/3 0/46 0/34	188 188	J. Fjelstad, T. DiStefano, B.Faraji, C. Mitchell, z Kovac, "mBGA Packaging Technology for Integrated Circuits," NEPCON East, June 1995 T.DiStefano, J. FJelstad,''Ctlip-scalc Packaging meets futuredesign nc&,''SolId State Technology, April 1996 *Gold bond ribbon Ducticle-copper bond ribbon survived 500 cycles
Wafer Level Redistribution 	0"(<> 1 00°C (Thermal Shock)	>2000 underfill <40 no under fiill	NA	266	R Chanchani, et al, "mini Ball Gird Array (mBGA) Assembly on MCM-I, Boards," Proceedings of Electronic Components and Technology Conference, May 18-21, 1997
Ceramic CSP 	-40°C <>125"(:	~600* no underfill, PWB0.6mm >900* no underfill, PWB1.6mm	NA	220	K. Ianzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Pethnology, " Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 *Private Communication

- Wafer package with the extreme CTE mismatch: Thermal cycling test results for assembly of a wafer redistributed package is shown in the Table 1. In this package a thin film nlctal/polymer redistributes the location of the solder bumps over the chip to make these compatible with the surface mount footprint. The height of the package type increases by the thickness of metal polymer layer from the bare chip. This additional layer will not generally absorb the CTE mismatch between the chip and board and therefore the assembly reliability of these package should bc very similar to C4 assemblies. Without materials, the assembled package failed less than 40 cycles when subjected to t hermal cycling bet ween 0°C and 100°C. For these types of packages, general ly underfilling is requi red to achieve acceptable level of assembly reliability. The underfilled assemblies did not failed to 2,000 cycles.

- Ceramic package with rigid interposer: The non-wafer level ceramic packages have shown reasonable assembly reliability with no underfilling. Thermal cycling results for a ceramic package on FR-4 is also included in the Table 1. The ceramic CSP uses the same design rules as mulilayer ceramic (MLC) with the first level interconnection choices of thermal compression and gold stud bump, solder flip chip, and wire bond. The strength, rigidity, coplanarity, and chamber of package arc excellent. The package assembly on a 0.6mm low Tg FR-4 were failed at about 600 thermal cycles between -40°C to 125°C. Cycles to failure increased to more than 900 cycles when PWB thickness increased to 1.6 mm. Thicker FR-4 is expected to show better rigidity when exposed to 125°C, temperature close to the low Tg FR-4 polymer used for this study.

Assembly Reliability for Conventional Packages and Those Projected for CSPs

Reliability of conventional SM packages as well as Bal I Grid Arrays have been investigated at JPL. Cycles to failure test data points and their Weibull distributions for 28-, and 20-pin I. CC, and 68-pin gull wing assemblies arc shown in Figure 2. Thermal cycling ranged from -55°C to 100°C with 246 minute duration. The failure distribution percentiles were approximated using a median plotting position, Fi = (i-0.3)/(n+0.4). The two-parameter Weibull cumulative failure distribution was used to fit data.

For comparison, projected cycles to failure for low count CSPS arc also included. Results arc those gathered from literature and projected based on a modified Coffin-Manson relationship. It is seen that board reliabilities of most CSP packages arc comparable or belter than their LCC counterparts. These packages. however. arc not as robust as leaded packages including gull wing and J-leads (data for J-leads arc not show in Figure I since there were no joint failures to 3,000 cycles).

Systematic Approach to Assess CSPS Board Reliability

Board reliability information is key element in Facilitating CSPs implementation in commercial and especially in high reliability applications. For wider applications of this technology, the potential user will need design reliability data for its design since often they have no resources, time, or ability to perform complex environmental characterizations. To help to build the infrastructure in these areas, JPL has formed a consortium with the objectives of addressing many technical issues regarding tbc interplay of package type, 1/0 counts, PWB materials, surface finish, and manufacturing variables for the quality and reliability of assembly packages, The JPL-led microtypeBGA consortium is now building its first test vehicle with sixteen packages from eleven manufacturers with 1/0s ranging from I 210540.

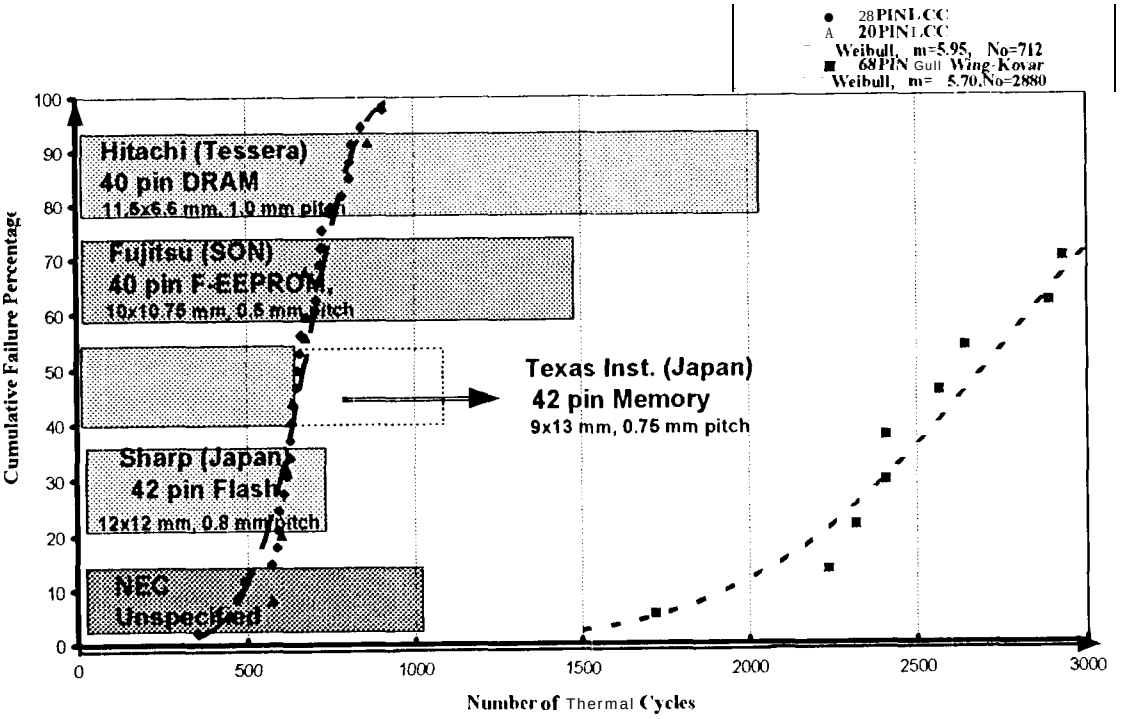


Figure 1. Projected Cycles to failures for Low Pin Count CSP Assemblies and Cumulative Failure Distributions for Conventional SM Package Assemblies Tested at JPL (-55°C to 100°C)

Conclusions

The JPL-led consortium is formed 10 address many board reliability issues of CSPS. Understanding of overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with these miniaturized packages arc key in collecting meaningful test results.

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About the Author

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering. At JPL, he supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored over 30 technical papers and numerous patentable innovations. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 all in engineering from University of California at Los Angeles (UCLA).